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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/923,207	08/06/2001	Eugene A. Fitzgerald	Amber.5739B	8977

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EXAMINER	
LINDSAY JR, WALTER LEE	
ART UNIT	PAPER NUMBER
2812	6

DATE MAILED: 05/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/923,207	Applicant(s) FITZGERALD ET AL.	
	Examiner Walter L. Lindsay, Jr.	Art Unit 2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-39 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-39 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3,5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Soref et al. U.S. Patent No. 6,154,475 in view of Pfiester U.S. Patent No. 5,166,084.

Soref discloses the formation of a $Si_{1-x}Ge_x$ layer and a $Si_{1-y}Ge_y$ layer.

The first step is to grow a graded index buffer layer 1, also known as a virtual substrate, upon the SOI/SOS platform 3, which includes silicon base 2, insulator 4 and silicon layer 6. The insulator could consist of sapphire, silicon dioxide or the like. This $Si_{1-x}Ge_x$ graded relaxed buffer layer 1 is relatively thick, approx 1-2mm, with a thickness larger than the critical thickness for stable strain, making this layer relaxed or strain-relieved. Its composition may vary linearly, or in steps, from Si up to $Si_{1-x}Ge_x$ where x is about 0.5, but could extend up to 60 percent Ge. This layer has very few defects per square-cm at its top surface, so its top surface presents an excellent surface for Ge and Si growth. The lattice parameter of the buffer is about 5.545, midway between Si and Ge. Fig. 1 shows the emitter-up geometry, although emitter-down geometry, mentioned below, is feasible.

In the emitter-up case, a highly doped 4-nm p-type $Si_{0.5}Ge_{0.5}$ stably strained layer 5, the collector contact of the laser, is grown upon the buffer. This is one of two

electrical contacts of the p-i-p diode. Following that, the undoped, strain-symmetric Ge-Si superlattice 7 is grown upon the collector 5. The superlattice (SL) constitutes the intrinsic region of the diode. In some cases the SL will be lightly doped to avoid space charge effects in the SL. The superlattice is constructed so that the layer adjacent to the p-SiGe collector 5 is a first Si layer 9, thin enough (1.0-1.5 nm) for tunneling from the SL to the collector. The top layer 11 of the SL is a second thin Si layer through which holes can thus tunnel into the active SL from the emitter 13. A heavily doped stably strained p-type $Si_{1-y}Ge_y$ emitter/injector layer 13, the second electrical contact, is grown upon the SL (y is roughly 0.5). The forward-biased p-i-p laser diode is capable of injecting carrier holes into an upper subband of the SL such as miniband-HH2. The emitter 13 would be a 10 to15 nm pseudomorphic layer (thickness <20 nm, the critical thickness for stable strain of the y alloy with respect to the x alloy, where y-x 0.1). Generally, a thin p+ injector layer is preferred to a "thick" layer such as 400 nm in thickness because the injector overlaps the tail of the guided mode, and a reduction in injector thickness reduces waveguide losses (the tail of the guided optical mode intersects a smaller volume of absorbing free carriers in a thinner layer). To reduce the optical attenuation effects produced by a metallic contact layer on top of the laser waveguide and directly on the p+ emitter 13, an optional dielectric spacer layer 17 can be interposed. This is a one micron thick lattice-matched p-type $Si_{0.5}Ge_{0.5}$ waveguide-cladding layer as shown. Finally, a conductive metal or poly-Si rectangular electrode 15 is deposited upon the top of the laser stack to be connected to voltage biasing source 21 as shown. With reactive ion etching or focused ion-beam etching, it is necessary to

etch the SL, the emitter, and the upper cladding into a strip-shape in order to form a strip optical waveguide for this laser (col. 4 lines 8-61).

Pfiester discloses the selective etching and removal of a silicon-germanium layer.

Fig. 1C depicts a germanium-silicon removal step for device 10. The masking layer 22 and the nitride layer 20 are used to dimension the channel size opening in the germanium-silicon layer 18. To accomplish the germanium-silicon etch, a wet etch solution comprising HF, H2O2 and CH3COOH respectively in a (1:2:3) ratio is used. It is important to note at this point that other newly discovered dry etches can also accomplish the germanium-silicon etch step. The previously mentioned wet etch step, outlined in a paper by G.K. Chang et. al , entitled "Selective Etching of SiGe on SiGe/Si Heterostructures" , University of California, Jan., 1991, the Electrochemical Society Inc., Vol. 138, No. 1, Page 202 etches germanium-silicon (SiGe) with an extremely high degree of selectively to exposed or underlying silicon layers (col. 4 lines 9-41).

In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the selective etching of a silicon-germanium layer as taught and described in Pfiester in the primary reference of Soref in order to selectively etch silicon germanium while not disturbing the underlying silicon layers.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (703) 306-5727. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John F Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 308-3325.

WLL
May 16, 2002

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800